What is claimed is:

1. An apparatus comprising:

an input transistor and a second transistor coupled as a Darlington pair; and

a bias circuit to increase a collector-to-emitter bias current in the first transistor.

2. The apparatus of claim 1 wherein the bias circuit comprises a voltage controlled current source.

3. The apparatus of claim 1 wherein the bias circuit comprises an operational amplifier coupled to maintain a substantially constant base voltage on the second transistor.

4. The apparatus of claim 1 further comprising a cascode transistor coupled between an upper power supply node and collectors of the input and second transistors.

5. The apparatus of claim 4 further comprising a second bias circuit to bias the cascode transistor.

6. The apparatus of claim 1 further comprising a third bias circuit to apply a bias voltage to a base of the input transistor.

7. The apparatus of claim 6 wherein the input transistor comprises a heterojunction bipolar transistor.

8. The apparatus of claim 6 wherein the input transistor comprises an Indium Phospate transistor.

9. The apparatus of claim 1 wherein the bias circuit comprises a digital-to-analog converter.

10. The apparatus of claim 1 further comprising an inductor coupled to a collector of the second transistor.

11. The apparatus of claim 1 further comprising an inductor coupled to an emitter of the second transistor.

12. An apparatus comprising:

an amplifier including an input transistor and a second transistor coupled as a Darlington pair;

a controllable bias circuit coupled to an emitter of the input transistor; and

a control circuit to influence operation of the controllable bias circuit.

13. The apparatus of claim 12 further comprising a second controllable bias circuit coupled to a base of the input transistor.

14. The apparatus of claim 12 wherein the controllable bias circuit comprises an operational amplifier coupled as an error amplifier.

15. The apparatus of claim 14 further comprising a low pass filter between an output of the operational amplifier and the emitter of the input transistor.

16. The apparatus of claim 12 wherein the control circuit includes a digital-to-analog converter.

17. The apparatus of claim 12 wherein the control circuit includes a processor.

18. The apparatus of claim 12 further comprising a cascode transistor coupled between an upper power supply node and a collector of the input transistor.

19. The apparatus of claim 18 further comprising a controllable bias circuit coupled to a control node of the cascode transistor.

20. The apparatus of claim 19 wherein the control circuit is coupled to influence operation of the controllable bias circuit for the cascode transistor.

21. The apparatus of claim 19 further comprising an automatic gain control circuit coupled between an output of the amplifier and the controllable bias circuit for the cascode transistor.

22. An electronic system comprising:

an antenna;

an amplifier coupled to the antenna, the amplifier including an input transistor and a second transistor coupled as a Darlington pair;

a controllable bias circuit coupled to an emitter of the input transistor; and

a control circuit to influence operation of the controllable bias circuit.

23. The electronic system of claim 22 further comprising a second controllable bias circuit coupled to a base of the input transistor.

24. The electronic system of claim 22 wherein the controllable bias circuit comprises an operational amplifier coupled as an error amplifier.

25. The electronic system of claim 22 wherein the control circuit comprises a processor.

26. A method comprising increasing a bias current in an input transistor of a Darlington pair by providing a current path from, and a voltage path to, an emitter of the input transistor.

27. The method of claim 26 further comprising:
applying a reference signal to a base of the input transistor; and
measuring an output voltage of the Darlington pair.

28. The method of claim 27 further comprising modifying a bias voltage applied to the base of the input transistor.

29. The method of claim 27 wherein increasing a bias current comprises changing a bias voltage on a voltage controlled current source.

30. The method of claim 27 further comprising modifying a bias voltage on a cascode transistor coupled between an upper power supply node and the Darlington pair.